

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): DODD, SIMON

Confirmation No.: 9553

Application No.: 10/055,161

Examiner: LATTIN, C.W.

Filing Date: Oct 26, 2001

Group Art Unit: 2812

Title: DEVICES AND METHODS FOR INTEGRATED CIRCUIT MANUFACTURING

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- (X) Response/Amendment () Petition to extend time to respond
() New fee as calculated below () Supplemental Declaration
() No additional fee (Address envelope to "Mail Stop Non-Fee Amendment")
() Other: (fee \$)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	6	MINUS	22	= 0	X \$18	\$ 0
INDEP. CLAIMS	1	MINUS	7	= 0	X \$84	\$ 0
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$280	\$ 0
EXTENSION FEE	1ST MONTH \$110.00	2ND MONTH \$410.00	3RD MONTH \$930.00	4TH MONTH \$1450.00		\$ 0
OTHER FEES						\$
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

Date of Deposit: Jul 3, 2003

Typed Name: Colette Angle-Olson

Signature: Colette Angle-Olson

Respectfully submitted,

DODD, SIMON

By

Peter Reitan

Attorney/Agent for Applicant(s)

Reg. No. 48,603

Date: Jul 3, 2003



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
DODD et al.)
)
Serial No.: 10/055,161) Group Art Unit: 2812
)
Filed: 10/26/2001) Examiner: LATTIN, C. W.
)
For: DEVICES AND METHODS FOR)
INTEGRATED CIRCUIT)
MANUFACTURING)
_____)

RESPONSE TO FINAL REJECTION (37 CFR 1.116(b))

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to an office action mailed May 22, 2003 in the above-referenced application and to a telephone message left by Examiner Lattin on July 2, 2003.

IN THE CLAIMS

Please cancel Claims 14-20, 23-31 and 33-35 without prejudice.

Please amend Claim 32 to read as follows:

32. (Amended) A process of making a multi-layered integrated circuit, comprising the steps of:
forming, at a surface of a semiconductor die, at least an insulating layer;

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